Weiwen Jiang

Postdoctoral Researcher
Department of Computer Science and Engineering
University of Notre Dame

Address: 254 Fitzpatrick Hall of Engineering, Notre Dame, IN 46556
Email: wjiang2@nd.edu
Tel: +1 (412)427-0695
Website: https://wjiang.nd.edu

Research Interests and Specialties

- **Machine Learning System Design and Optimization:** especially for the co-exploration of neural architectures and hardware design [1][2][4][5][6][8][25][26][27][28][29].
- **General Embedded System Design and Optimization:** especially for (1) heterogeneous pipelined MPSoCs [3][10][30][31][37][40]; (2) asynchronous embedded systems [12][13][32][33][34][36]; (3) NoC-based MPSoCs [15][16][17][18] [39][45][46][48][54]; and (4) distributed systems [12][44][53].
- **Emerging Techniques:** especially for non-violate memory based system design and optimization [5][7][11][19][20][21][22][23][24][35][38][41][42][43][47] [49][50][51][52].

Employment

University of Notre Dame (PI: Dr. Yiyu Shi) JUN. 2019 – NOW. NOTRE DAME, U.S.
- **Postdoctoral Researcher in the Department of Computer Science and Engineering**. Focus on the co-exploration of neural architectures and hardware design, including qauntum computer.

University of Notre Dame JAN. 2020 – MAY. 2020 NOTRE DAME, U.S.
- **Teaching Assisitant**. CSE20221, Logical Design.

East China Normal University APR. 2019 – APR. 2020 SHANGHAI, CHINA
- **Guest Research Fellows** in Big Data and Intelligent System Lab.

University of Pittsburgh (PI: Dr. Jingtong Hu) OCT. 2018 – JUN. 2019 PITTSBURGH, U.S.
- **Research Scholar**. Focus on the co-exploration of neural architecture and hardware design

Education

University of Pittsburgh (PI: Dr. Jingtong Hu) OCT. 2017 – SEP. 2018 PITTSBURGH, U.S.
- **Joint Ph.D. program in the Department of Electrical and Computer Engineering**. Focus on the design of heterogeneous computing platforms for neural networks.

Chongqing University (Advisor: Dr. Edwin Sha) SEP. 2013 – JUN. 2019 CHONGQING, CHINA
- **Ph.D. degree in Computer Science**. Focus on the embedded system design and optimizations: designing high-performance and low-cost heterogeneous pipelining systems.

Nanjing Agriculture University SEP. 2008 – JUN. 2012. JIANGSU, CHINA
- **Bachelor degree in Computer Science**. Major in Network Engineering.

Awards

Best Paper Nomination in ASP-DAC 2020 (12 out of 263 submissions) 01/2020. BEIJING

Best Paper Nomination in CODES+ISSS 2019 (3 out of 74 submissions) 10/2019. NEW YORK

Best Paper Nomination in DAC 2019 (5 out of 815 submissions)	06/2019. LAS VEGAS
Best Paper Award in ICCD 2017 (5 out of 258 submissions)	11/2017. BOSTON
Best Student Paper in ESTC 2017	11/2017. CHINA
Best Paper Nomination in ASP-DAC 2016	01/2016. MACAO
Best Paper Award in NVMSA 2015	08/2015. HONGKONG
Editor's pick of the year 2016 in IEEE TC	12/2016. USA
China National Scholarship (1% among all postgraduate students)	11/2017. CHINA

Research & Other Grants

1. PI, 100%, "Hardware/Software Co-Exploration for Machine Learning on Edge", from NSF IUCRC ASIC center, 10/01/19 - 09/30/20, $100,000
2. PI, 100%, Chinese Government Scholarship to Visit University of Pittsburgh (201706050116), 10/01/17 - 09/30/18, $30,000
3. Co-PI, "Software Defined FPGA Hardware and Co-Exploration for Real-Time Applications", IBM & University of Notre Dame Quantum program, 11/01/19 - now, accessing to IBM Q system
4. Research Opportunities Week (ROW) at the Technical University of Munich (TUM), 04/20/2020-04/27/2020
5. IEEE Council on Electronic Design Automation (CEDA) for ESWEEK'19, $1,000
6. Grants from ACM SIGDA to participate the HALO workshop in ICCAD'19
7. Travel grants from ACM to attend FPGA'19
8. Scholarship from SIGDA and IEEE CEDA to attend PhD Forum at DAC'18
9. Scholarship from SIGDA and Microsoft to participate Student Research Competition at ICCAD'17

Teaching Experience

High-Performance Parallel Computing (TA for Dr. Edwin Sha)	2014 – 2015. CHONGQING UNIV.
INVESTING NOW summer program (Volunteer)	JULY 2018. UNIV. OF PITTSBURGH.
Striving for Excellence in Teaching (Certificate)	2019 – NOW. UNIV. OF NOTRE DAME.
Logic Design and Sequential Circuits (CSE20221)	JAN – MAY 2020. UNIV. OF NOTRE DAME
Machine Learning for Embedded Systems (CSE60685)	JAN – MAY 2020. UNIV. OF NOTRE DAME

Mentor of Students

- Hailiang Dong (Master) [3][11][31][37][40][42], First Employer: Ph.D in University of Texas at Dallas
- Xinchi Li (Master) [42], First Employer: Tencent in Chengdu
- Yutong Liang (Master) [44], First Employer: PingCAP Inc. in Beijing
- Zhulin Ma (Ph.D. candidate) [11][19]
- Xinyi Zhang (Ph.D. candidate in University of Pittsburgh) [1][2][28]
- Qing Lu (Ph.D. candidate in University of Notre Dame) [26][29]
- Zheyu Yan (Ph.D. candidate in University of Notre Dame) [5][25]

Refereed Publications

Three Representative Papers

[1] **W. Jiang**, X. Zhang, E. H.-M. Sha, L. Yang, Q. Zhuge, Y. Shi, and J. Hu, "Accuracy vs. Efficiency: Achieving Both through FPGA-Implementation Aware Neural Architecture Search," *Proc. Design Automation Conference* (***DAC***), Las Vegas, NV, USA, June. 2019. (**BEST PAPER NOMINATION**)

[2] **W. Jiang**, E. H.-M. Sha, X. Zhang, L. Yang, Q. Zhuge, Y. Shi and J. Hu, "Achieving Super-Linear Speedup across Multi-FPGA for Real-Time DNN Inference", International Conference on Hardware/Software Co-design and System Synthesis (CODE+ISSS@New York), also appears at ACM Transactions on Embedded Computing Systems (TECS), 2019. (**BEST PAPER NOMINATION**)

[3] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, H. Dong and X. Chen, "On the Design of Minimal-Cost Pipeline Systems Satisfying Hard/Soft Real-Time Constraints," *IEEE International Conference on Computer Design* (***ICCD@Boston***) and *in IEEE Transactions on Emerging Topics in Computing* (***TETC***), Jan. 2018. (**BEST PAPER AWARD**)

Under Review

[4] **W. Jiang**, L. Yang, E. H.-M Sha, Q. Zhuge, S. Gu, Y. Shi and J. Hu, "Hardware/Software Co-Exploration of Neural Architectures", *submitted to IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***).

[5] **W. Jiang**, Q. Lou, Z. Yan, L. Yang, J. Hu, X. Hu, and Y. Shi, "Device-Circuit-Architecture Co-Exploration for Computing-in-Memory Neural Accelerators", *submitted to IEEE Transactions on Computers* (***TC***).

[6] Q. Lu, **W. Jiang**, X. Xu, and Yiyu Shi, "Weightless Neural Architecture Search: Rethinking Quantization-Aware Training of Neural Networks", *submitted to International Conference on Machine Learning* (***ICML***).

Journal Paper

[7] **W. Jiang**, B. Xie, C-C Liu and Y. Shi, "Integrating Memristors and CMOS for Better AI", *accepted by Nature Electronics* (*News and Views*), Sep. 2019

[8] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "Heterogeneous FPGA-based Cost-Optimal Design for Timing-Constrained CNNs", *accepted by CASES 2018* (*in ESWEEK*) and *appear in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***).

[9] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, L. Yang, X. Chen and J. Hu, "On the Design of Time-Constrained and Buffer-Optimal Self-Timed Pipelines", *in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (***TCAD***), May. 2018.

[10] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Yang, L. Zhou and Q. Zhuge, "Optimal Functional-Unit Assignment for Heterogeneous Systems under Timing Constraint," *in IEEE Transactions on Parallel and Distributed Systems* (***TPDS***), 28(9): 2567-2580, 2017.

[11] E. H.-M. Sha, **W. Jiang**, H. Dong, Z. Ma, R. Zhang, X. Chen and Q. Zhuge, "Towards the Design of Efficient and Consistent Index Structure with Minimal Write Activities for Non-Volatile Memory", *in IEEE Transactions on Computers* (***TC***), 67(3): 432-448, 2018.

[12] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and Lin Wu, "Efficient Assignment Algorithms to Minimize Operation Cost for Supply Chain Networks in Agile Manufacturing," *in Computers & Industrial Engineering*, 108: 225-239, 2017.

[13] **W. Jiang**, E. H.-M. Sha, X. Chen, L. Wu and Q. Zhuge, "Synthesizing Distributed Pipelining Systems with Timing Constraints via Optimal Functional Unit Assignment and Communication Selection," *in Journal of Computational Science*, 26: 332-343, 2018.

[14] **W. Jiang**, Q. Zhuge, X. Chen, L. Yang, J. Yi and E. H.-M. Sha, "Properties of Self-Timed Ring Architectures for Deadlock-Free and Consistent Configuration Reaching Maximum Throughput," *in Journal of Signal Processing Systems*, 84(1): 123-137, 2016.

[15] W. Liu, L. Yang, **W. Jiang**, L. Feng, N. Guan, W. Zhang and N. Dutt, "Thermal-aware Task Mapping on Dynamically Reconfigurable Network-on-Chip based Multiprocessor System-on-Chip", *in IEEE Transactions on Computers* (***TC***), 2018.

[16] L. Yang, W. Liu, **W. Jiang**, M. Li, P. Chen and E. H.-M. Sha, "FoToNoC: A Folded Torus-Like Network-on-Chip based Many-Core Systems-on-Chip in the Dark Silicon Era," *in IEEE Transactions on Parallel and Distributed Systems*, Dec. 2016. DOI:10.1109/TPDS.2016.2643669.

[17] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H. M. Sha, "Application Mapping and Scheduling for Network-on-Chip-Based Multiprocessor System-on-Chip With Fine-Grain Communication Optimization" *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 24(10): 3027-3040, Oct. 2016.

[18] L. Yang, W. Liu, **W. Jiang**, C. Chen, M. Li, P. Chen and E. H.-M. Sha, "Hardware-software collaboration for dark silicon heterogeneous many-core systems," *in Future Generation Computer systems*, 68: 234-247, 2017.

[19] Z. Ma, E. H.-M. Sha, Q. Zhuge, **W. Jiang**, R. Zhang and S. Gu, "Towards the design of efficient hash-based indexing scheme for growing databases on non-volatile memory," *in Future Generation Computer systems*, Sep. 2019.

[20] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "A New Design of In-Memory File System Based on File Virtual Address Framework," *in IEEE Transactions on Computers*, 65(10):2959-2972, Oct. 2016.

[21] X. Chen, E. H.-M. Sha, **W. Jiang**, C. Yang, T. Wu and Q. Zhuge, "Refinery swap: An efficient swap mechanism for hybrid DRAM-NVM systems," *in Future Generation Computer systems*, 2017.

[22] X. Chen, E. H.-M. Sha, Q. Zhuge, **W. Jiang**, J. Chen and J. Xu A unified framework for designing high performance in-memory and hybrid memory file systems *Journal of Systems Architecture - Embedded Systems Design*, 68: 51-64, 2016.

[23] X. Chen, E. H.-M. Sha, Q. Zhuge, C. J. Xue, **W. Jiang** and Y. Wang, "Efficient data placement for improving data access performance on domain-wall memory" *IEEE Transactions on Very Large Scale Integration* (*VLSI*) *Systems*, 24(10): 3094-3104, 2016.

[24] P. Dai, Q. Zhuge, X. Chen, **W. Jiang** and E. H.-M. Sha, "Effective file data-block placement for different types of page cache on hybrid main memory architectures," *in Design Automation for Embedded Systems*, 17(3-4): 485-506, 2013.

Conference Paper

[25] L. Yang, Z. Yan, M. Li, H. Kwon, L. Lai, T. Krishna, V. Chandra, **W. Jiang***, Y. Shi, "Co-Exploration of Neural Architectures and Heterogeneous ASIC Accelerator Designs Targeting Multiple Tasks", *Proc. Design Automation Conference* (***DAC***), San Francisco, CA, July 19-23. (* cor. author)

[26] S. Bian, **W. Jiang**, Q. Lu, Y. Shi, and T. Sato, "NASS: Optimizing Secure Inference via Neural Architecture Search", *submitted to 24th European Conference on Artificial Intelligence* (***ECAI'20***)

[27] L. Yang*, **W. Jiang***, W. Liu, E. H.-M. Sha, Y. Shi and J. Hu, "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence," *Proc. Asia and South Pacific Design Automation Conference* (***ASP-DAC***), Beijing, Jan. 2020. (**BEST PAPER NOMINATION**, * equal contribution)

[28] X. Zhang, **W. Jiang**, Y. Shi and J. Hu, "When Neural Architecture Search Meets Hardware Implementation: from Hardware Awareness to Co-Design," *Proc. IEEE Computer Society Annual Symposium on VLSI* (*ISVLSI*), Miami, Florida, USA, Aug. 2019. (Invited Paper)

[29] Q. Lu, W. Jiang, X. Xiao, J. Hu and Y. Shi, "On Neural Architecture Search for Resource-Constrained Hardware Platforms," *Proc. IEEE/ACM International Conference On Computer-Aided Design* (*ICCAD*), Westminster, CO, 2019. (Invited paper)

[30] **W. Jiang**, E. H.-M. Sha, Q. Zhuge and X. Chen, "Optimal Functional-Unit Assignment and Buffer Placement for Probabilistic Pipelines," *Proc. International Conference on Hardware/Software Co-design and System Synthesis* (***CODES+ISSS***), Pittsburgh, PA, USA, Oct. 2016.

[31] **W. Jiang**, E. H.-M. Sha, Q. Zhuge, H. Dong and X. Chen, "Optimal Functional Unit Assignment and Voltage Selection for Pipelined MPSoC with Guaranteed Probability on Time Performance," *Proc. Languages, Compilers, and Tools for Embedded Systems* (***LCTES***), Barcelona, Spain, Jun. 2017.

[32] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, L. Yang and X. Chen, "On the Design of High-Performance and Energy-Efficient Probabilistic Self-Timed Systems," *Proc. High Performance Computing and Communications* (***HPCC***), NewYork, NY, USA, Aug. 2015.

[33] E. H.-M. Sha, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "Prevent Deadlock and Remove Blocking for Self-Timed Systems," *Proc. International Conference on Algorithms and Architectures for Parallel Processing* (***ICA3PP***), Zhangjiajie, China, Nov. 2015.

[34] **W. Jiang**, E. H.-M. Sha, X. Chen, Q. Zhuge and L. Wu, "Optimal Functional Assignment and Communication Selection under Timing Constraint for Self-Timed Pipelines," *Proc. IEEE International Conference on Embedded Software and Systems* (***ICESS***), Chengdu, China, Aug. 2016.

[35] X. Chen, E. H.-M. Sha, Z. Sun, Q. Zhuge and **W. Jiang**, "The Design and Implementation of an Efficient Data Consistency Mechanism for In-Memory File Systems," *Proc. IEEE International Conference on Embedded Software and Systems* (***ICESS***), Chengdu, China, Aug. 2016.

[36] **W. Jiang**, Q. Zhuge, J. Yi, L. Yang and E. H.-M. Sha, "On self-timed ring for consistent mapping and maximum throughput," *Proc. Embedded and Real-Time Computing Systems and Applications* (***RTCSA***), Chongqing, China, Aug. 2014.

[37] E. H.-M. Sha, H. Dong, **W. Jiang**, Q. Zhuge, X. Chen and L. Yang, "On the Design of Reliable Heterogeneous Systems via Checkpoint Placement and Core Assignment," *Proc. Great Lakes Symposium on VLSI* (*GLSVLSI*), Chicago, IL, USA, May. 2018.

[38] X. Chen, E. H.-M. Sha, Y. Zeng, C. Yang, **W. Jiang** and Q. Zhuge, "Efficient wear leveling for inodes of file systems on persistent memories," *Proc. Design, Automation & Test in Europe Conference & Exhibition* (*DATE*), Dresden, Germany, Mar. 2018.

[39] W. Liu, L. Yang, **W. Jiang** and N. Guan, "Work In Progress : Communication Optimization for Thermal Reliable Many-core Systems," *Proc. International Conference on Hardware/Software Co-design and System Synthesis* (***CODES+ISSS***), Seoul, South Korea, Oct. 2017.

[40] H. Dong, E. H.-M. Sha, **W. Jiang**, X. Chen, R. Zhang and Q. Zhuge, "Towards the Design of Optimal Range Assignment for Elevator Groups under Fluctuant Traffic Loads," *Proc. Embedded and Real-Time Computing Systems and Applications* (***RTCSA***), Hsinchu, Taiwan, Aug. 2017.

[41] X. Chen, E. H.-M. Sha, A. Abdulah, Q. Zhuge, L. Wu, C. Yang and **W. Jiang**, "The Design and Implementation of an Efficient User-space In-memory File System," *Proc. IEEE Non-Volatile Memory System and Applications Symposium* (***NVMSA***), Hsinchu, Taiwan, Aug. 2017.

[42] X. Li, Q. Zhuge, **W. Jiang**, H. Dong, W. Lin, X. Chen and E. H.-M. Sha, "A Research of Reducing Write Activities in Multi-table Join for Non-Volatile Memories," *Proc. 15th CCF Annual Conference on Embedded Systems* (*ESTC*), Shenyang, China, Nov. 2017. (**BEST STUDENT PAPER AWARD**)

[43] X. Chen, E. H.-M. Sha, **W. Jiang**, Q. Zhuge, J. Chen, J. Qin, Y. Zeng, "The Design of an Efficient Swap Mechanism for Hybrid DRAM-NVM Systems," *Proc. International Conference on Embedded Software* (***EMSOFT***), Pittsburgh, PA, USA, Oct. 2016.

[44] E. H.-M. Sha, Y. Liang, **W. Jiang**, X. Chen and Q. Zhuge, "Optimizing Data Placement of MapReduce on Ceph-Based Framework under Load-Balancing Constraint," *Proc. International Conference on Parallel and Distributed Systems* (***ICPADS***), Wuhan, China, Dec. 2016.

[45] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Yi and E. H.-M. Sha, "FoToNoC: A hierarchical management strategy based on folded lorus-like Network-on-Chip for dark silicon many-core systems,"

Proc. 2016 21st Asia and South Pacific Design Automation Conference (***ASP-DAC***), Macao, Jan. 2016. (**BEST PAPER NOMINATION**)

[46] L. Yang, W. Liu, **W. Jiang**, M. Li, J. Wang, "Isolation of Physical and Logical Views of Dark-Silicon Many-Core Systems for Reliability and Performance Co-Optimization", *Embedded System Technology*, Springer Singapore, 2015.

[47] X. Chen, E. H.-M. Sha, Q. Zhuge, P. Dai and **W. Jiang**, "Optimizing data placement for reducing shift operations on domain wall memories," *Proc. Design Automation Conference* (***DAC***), San Francisco, California, USA, Jun. 2015.

[48] L. Yang, W. Liu, **W. Jiang**, W. Zhang, M. Li, J. Yi, D. Liu and E. H.-M. Sha, "Traffic-Aware Application Mapping for Network-on-Chip Based Multiprocessor System-on-Chip," *Proc. High Performance Computing and Communications* (***HPCC***), NewYork, NY, USA, Aug. 2015.

[49] E. H.-M. Sha, Y. Jia, X. Chen, Q. Zhuge, **W. Jiang** and J. Qin "The Design and Implementation of an Efficient User-space In-memory File System," *Proc. the 5th IEEE Non-Volatile Memory System and Applications Symposium* (***NVMSA***), Daegu, Korea, Aug. 2016.

[50] Z. Liu, E. H.-M. Sha, X. Chen, **W. Jiang**, and Q. Zhuge "Performance Optimization for In-Memory File Systems on NUMA Machines," *Proc. International Conference on Parallel and Distributed Computing, Applications and Technologies* (*PDCAT*), Guangzhou, China, Dec. 2016.

[51] E. H.-M. Sha, J. Chen, X. Chen, **W. Jiang**, and Q. Zhuge "The Design and Implementation of a High-Performance Hybrid Memory File System," *Proc. International Conference on Advanced Cloud and Big Data* (*CDB*), Chengdu, China, Dec. 2016.

[52] E. H.-M. Sha, X. Chen, Q. Zhuge, L. Shi and **W. Jiang**, "Designing an Efficient Persistent In-Memory File System," *Proc. the 4th IEEE Non-Volatile Memory System and Applications Symposium* (***NVMSA***), Hongkong, Aug. 2015. (**BEST PAPER AWARD**)

[53] J. Yi, W. Liu, **W. Jiang**, M. Qin, L. Yang, D. Liu, C. Xiao, L. Du and E. H.-M. Sha, "An Improved Thermal Model for Static Optimization of Application Mapping and Scheduling in Multiprocessor System-on-Chip," *Proc. IEEE Computer Society Annual Symposium on VLSI* (***ISVLSI***), Tampa, Florida, USA, Jul. 2014.

[54] L. Yang, W. Liu, **W. Jiang**, J. Yi, D. Liu and Q. Zhuge, "Contention-aware task and communication co-scheduling for network-on-chip based Multiprocessor System-on-Chip," *Proc. Embedded and Real-Time Computing Systems and Applications* (***RTCSA***), Chongqing, China, Aug. 2014.

Professional Services

Journal Reviewer

- IEEE Transactions on Computers (TC)
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- IEEE Transactions on Very Large Scale Integration (TVLSI)
- IEEE Transactions on Emerging Topics in Computing (TETC)
- IEEE Transactions on Neural Networks and Learning Systems (TNNLS)
- IEEE Embedded System Letter (ELS)
- IEEE Access
- ACM Transactions on Embedded Computing Systems (TECS)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- ACM Journal on Emerging Technologies in Computing (JETC)
- Journal of Computer Science and Technology (JCST)

- Communications in Statistics - Simulation and Computation
- Microprocessors and Microsystems (MICPRO)
- SPRINGER Journal of Signal Processing Systems (JSPS)
- HINDAWI Complexity (Complexity)

Conference Technical Program Committee:

- Late Break Results in Design Automation Conference (DAC 2020)
- IEEE Computer Society Annual Symposium on VLSI (ISLVLSI 2020)
- ACM Great Lakes Symposium on VLSI (GLSVLSI 2020)
- Student Research Forum at Asia and South Pacific Design Automation Conference (ASP-DAC 2020)
- 35th ACM/SIGAPP Symposium On Applied Computing (SAC 2020)
- 40th IEEE Real-Time Systems Symposium (RTSS 2019, Artifact Evaluation Committee)

Conference Review

- Reviewer of 2019 MICCAI Workshop on Hardware Aware Learning for Medical Imaging and Computer Assisted Intervention
- Design Automation Conference 2018, 2019, Expert Reviewers (DAC)
- International Conference on Compilers, Architecture, and Synthesis for Embedded Systems 2018, External Reviewer (CASES)

References on Request

- **Yiyu Shi** (yshi4@nd.edu), Associate Professor, University of Notre Dame, Notre Dame, IN, USA
  `Site Director of NSF I/UCRC ASIC Center`
  `Website: https://www3.nd.edu/~scl/index.html`
- **Jingtong Hu** (jthu@pitt.edu). Assistant Professor, University of Pittsburgh, PA, USA.
  `Website: http://pitt.edu/~jthu/`
- **Edwin H.-M. Sha** (edwinsha@cs.ecnu.edu.cn), Distinguished Professor, East China Normal University, Shanghai, China.
  `Changjiang Scholar, National Thousand People Plan Specially-invited Expert`
  `Website: https://faculty.ecnu.edu.cn/s/3741/t/37453/main.jspy`
- **Tei-wei Kuo** (teiwkuo@cityu.edu.hk), Professor, City University of Hong Kong, Kowloon, Hong Kong.
  `IEEE Fellow and ACM Fellow, Dean of College of Engineering`
  `Website: http://www.cityu.edu.hk/stfprofile/teiwei.kuo.htm`
- **Nikil Dutt** (dutt@ics.uci.edu). Chancellor's Professor, University of California, Irvine, CA, USA.
  `IEEE Fellow and ACM Fellow`
  `Website: https://www.ics.uci.edu/~dutt/`